VLSI Architectures (Sem -2: AY 2024-25)

Lab-8

**Objective:**

To understand, simulate, synthesize and characterize the combinatorial logic of EXECUTE Stage of the 5-stage pipelined implementation of RISC-V (RV32I) ISA.

A behavioral Verilog module for the combinatorial logic of the EXECUTE Stage is being provided to you.

(1) Check out this module for its logical correctness and syntactical correctness. Make corrections in the module as necessary and document the same.

(5) Then verify the design’s functionality through simulation. Synthesize the design and tabulate your synthesis results: LUT count, delay and power